Open XR Optics 400G Optical Module Form Factor Hardware Specifications

OXR.TCVRFFHW.01.0 Open XR Optics 400G Optical Module Form Factor Hardware Specifications
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ABSTRACT:

This document provides specifications for Open XR Optics compliant coherent transceiver modules that can transmit/receive up to 400Gbps. It provides specifications for the form factor related mechanical and management interfaces requirement of Open XR Optics modules to enable multi-vendor interoperable implementations.

The Open XR Optics Forum
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Open XR Optics Forum

The Open XR Optics Forum is the multi-source agreement (MSA) working group for XR optics, the industry's first point-to-multipoint coherent pluggable transceiver technology. The Open XR Optics Forum's mission is to foster collaboration that will advance development of XR optics-enabled products and services, accelerate adoption of intelligent coherent transceivers ,coherent point-to-multipoint network architectures, and drive standardization of networking interfaces to ensure ease of multi-vendor interoperability and an open, multi-source solution ecosystem.

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1. Scope

This document provides specification for Open XR compliant coherent transceiver modules. It focusses on mechanical and management interfaces with the objective of enabling the development of Multi Vendor Inter-Operable (MVIO) XR modules.

Form factor dependent specifications, for example, module pad configuration, are provided in dedicated sections of this document. This specification references other MSAs and standards, compliant implementations MUST adhere to of those as required by this specification.

This specification is for a 400G XR module but allows that to be configured as a 300G, 200G, or 100G module.

2. Introduction

Open XR optical modules are intelligent devices. Figure 1 is a functional block diagram of an XR module. There are two main components in the module: the DSP ASIC and TROSA, the figure illustrates the functionality of the supporting peripheral components and the communication channels required between them. Note that this is a conceptual diagram, not a reference design. Actual implementations may be different.

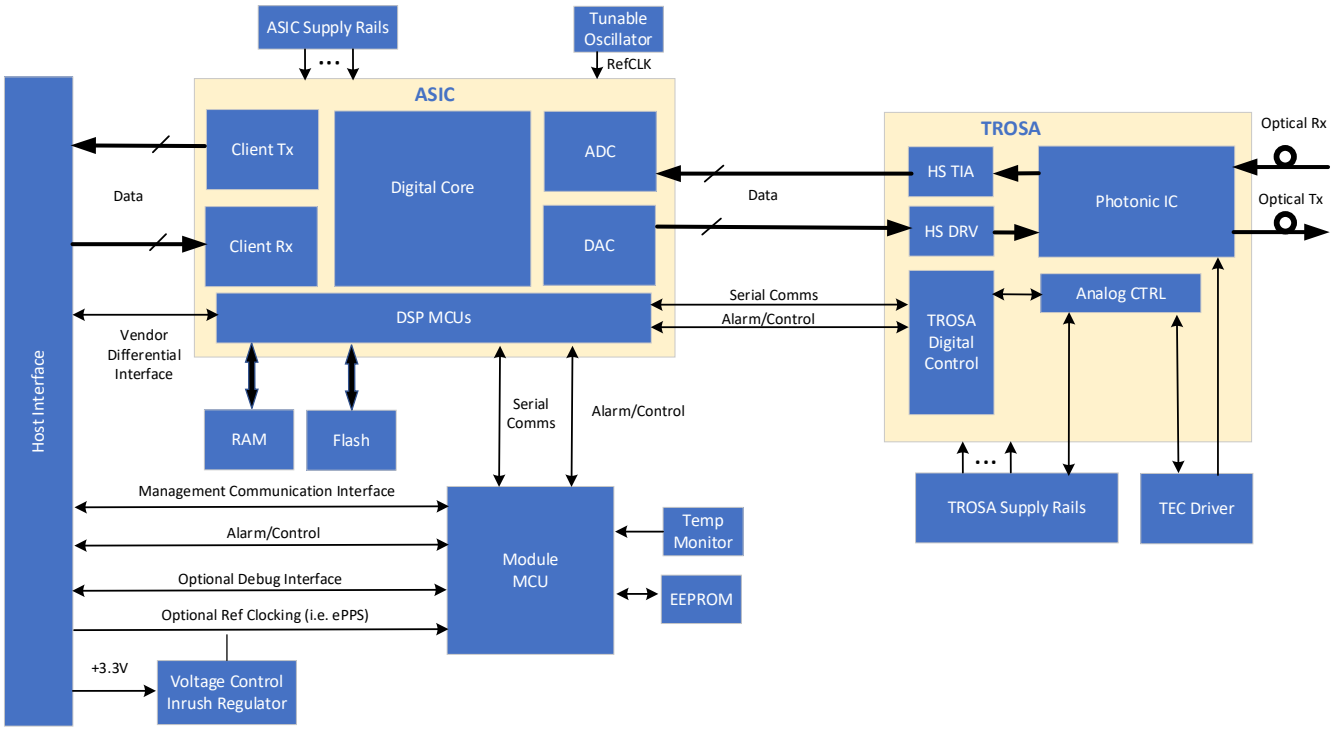

Figure 1. XR Optics Module Functional Block Diagram

3. XR Hardware Specifications

3.1 Electrical Interface Pad Layout and Function Description (Form Factor Dependent)

An Open XR module can be implemented in a variety of pluggable form factors. Open XR module shall comply with form factor specific pad assignment and functionalities, high speed and low speed electrical interface, mechanical dimensions and tolerance, module compliance standards, etc., as specified by the appropriate MSA.

This specification references QSFP-DD [1] and CFP2 [5] [6] form factors and electrical interface definitions including SGMII specifications. Some form factors have only limited pads and, in those cases, some Open XR features may not be supported.

3.1.1 QSFP-DD

Open XR QSFP-DD pad assignment is based on the QSFP-DD Hardware MSA definition [1] a compliant Open XR module shall follow the MSA pad definition, in addition, an Open XR QSFP-DD module uses the 4 Vendor Specific pads (46,47,49,50) as an SGMII interface. Those pins are assigned for SGMII Input p/n and SGMII Output p/n using Current Mode Logic (CML) for signaling (See Table 1). A more detailed description of the SGMII interface is in Section 3.3.

RxLOS (28) and TxDis (31) functions are optional. ePPS/Clock (69) is also optional; there is no plan to support ePPS/Clock by current 400G XR DSP/ASIC.

NC or Reserved pads are for future use. They may be used for debug or testing purposes but when not in use, these pads must be terminated as per MSA requirements. The rest of the pads follow the MSA definitions.

Pad	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	

26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46*	CML-I	SGMII_Module_IN_N (MSA: P/VS4)	SGMII Module Input differential pair *Open XR pad definition	3A	3
47*	CML-I	SGMII_Module_IN_P (MSA: P/VS1)	SGMII Module Input differential pair * Open XR pad definition	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49*	CML-O	SGMII_Module_OUT_N (MSA: P/VS2)	SGMII Module Output differential pair * Open XR pad definition	3A	3
50*	CML-O	SGMII_Module_OUT_P (MSA: P/VS3)	SGMII Module Output differential pair * Open XR pad definition	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future Use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVVMOS-I	ePPS/Clock	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	

75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1
Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal- common ground plane. Each connector Gnd contact is rated for a steady state current of 500mA.					
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.					
Note 3: Reserved and no Connect pads recommended to be terminated with 10 kOhm to ground on the host. Pad 65 may get terminated with 10 kOhm to ground on the host.					
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A, 3B.					
Note 5: TxDIS and RxLOS are not currently supported.					

Table 1. QSFP-DD Pad Assignment Table

3.1.2 CFP2

Open XR CFP2 pad assignment is based on the CFP2 Hardware MSA spec [5] and OIF CFP2 DCO Implementation Agreement [6] definition. Open XR CFP2 uses the 4 Vendor Specific input/output pads (Bottom side 2, 3, 5 ,6) for SGMII interface using CML for signaling. This is a deviation from the CFP2 HW MSA

Reference Clock pads (Top side 78, 79) are not used.

Rx_MCLK pads (Bottom 50, 51) are not used. These pins can be used for debug or testing purposes but when not in use, they must be terminated as per MSA requirements.

There are four more vendor specific pads that are not defined by Open XR (15,16,47,48). They are for vendor specific use, and must follow the MSA for termination requirements.

Bottom Row Pads

Pad	Name	I/O	Logic	Description
1	GND			
2*	OHIO_SGMII_RDn	**O**	CML	OHIO Module to Host *Open XR pad definition
3*	OHIO_SGMII_RDp	**O**	CML	OHIO Module to Host * Open XR pad definition
4	GND			
5*	OHIO_SGMII_TDn	**I**	CML	OHIO Host to Module * Open XR pad definition
6*	OHIO_SGMII_TDp	**I**	CML	OHIO Host to Module * Open XR pad definition
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage

11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	**I/O**		Module Vendor I/O A.
16	VND_IO_B	**I/O**		Module Vendor I/O B.
17	PRG_CNTL1	**I**	3.3V LVCMOS w/PUR	MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1"or NC: enabled
18	PRG_CNTL2	**I**	3.3V LVCMOS w/PUR	MSA Default: Hardware Interlock LSB "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W = not used
19	PRG_CNTL3	**I**	3.3V LVCMOS w/PUR	MSA Default: Hardware Interlock MSB "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W = not used
20	PRG_ALRM1	**O**	3.3V LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
21	PRG_ALRM2	**O**	3.3V LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
22	PRG_ALRM3	**O**	3.3V LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND			
24	TX_DIS	**I**	3.3V LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	**O**	3.3V LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	**I**	3.3V LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	**O**	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host.
28	MOD_RSTn	**I**	3.3V LVCMOS w/PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module (Full module reset)
29	GLB_ALRMn	**O**	3.3V LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	**I**	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-(2012)

32	MDIO	**I/O**	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	**I**	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	**I**	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	**I**	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	**I/O**		Module Vendor I/O C
37	VND_IO_D	**I/O**		Module Vendor I/O D
38	VND_IO_E	**I/O**		Module Vendor I/O E
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			3.3V Module Supply Voltage
43	3.3V			3.3V Module Supply Voltage
44	3.3V			3.3V Module Supply Voltage
45	3.3V_GND			
46	3.3V_GND			
47	Vendor_In1n	**I**	CML	Open XR does not specify this pad. It can be defined for vendor use
48	Vendor_In1p	**I**	CML	Open XR does not specify this pad. It can be defined for vendor use
49	GND			
50	RX_MCLKn or Vendor_Out1n	**O**	CML	Open XR does not specify this pad. It can be defined for vendor use
51	RX_MCLKp or Vendor_Out1p	**O**	CML	Open XR does not specify this pad. It can be defined for vendor use
52	GND			

Top Row Pads

Pad	Name	I/O	Logic	Description
79	REFCLKn	**I**	CML	Not required
78	REFCLKp	**I**	CML	Not required
Multiple	GND			
Multiple	RXp, RXn	**O**	CML	Module high speed data Output
Multiple	TXp, TXn	**I**	CML	Module high speed data Input

Table 2. CFP2 Pad Assignment Table

3.2 Module Power Supply Requirement and Environmental Maximum Ratings

Specifications in this section are applicable over the module's life, under full operating conditions and temperature range.

3.2.1 Module Power Supply Requirement

Parameter	Symbol	Min	Typical	Max	Unit	Condition
+3.3V Supply Voltage	Vcc	3.135	3.3	3.465	V	Host Voltage requirement at module interface pads
+3.3V Supply Current	Icc			Design Specific	A	See Note
Power Dissipation (0C to 70C Case temperature, over lifetime)	Pdiss			Design Specific	W	See Note
Low Power Mode Power Dissipation	LP-Pdiss			1.5	W	QSFP-DD
				2.0		CFP2

Table 3. Module Power Supply Requirement

Note: Different XR compatible devices may have different power dissipation ratings based on applications. Vendors should characterize and specify module power and current rating.

3.2.2 Power Supply Transient Requirement

XR module power supply transient behavior should follow the QSFP-DD Hardware MSA specified transient current tolerance. It specifies the Instantaneous Peak Current and Sustained Peak Current during transient states, and the limits for the Instantaneous Peak Current and Sustained Peak Current during the transient. The rating is based on module total power consumption. Detail can be found in QSFP-DD Hardware MSA [1]. The calculation of Instantaneous Peak Current and Sustained Peak Current are as follows.

Parameter	Symbol	Max	Unit
Instantaneous Peak Current	Icc_ip	Pdiss/2.5	A
Sustained Peak Current	Icc_sp	Pdiss/3.03	A

Table 4. Module Power Supply Transient Current Requirement

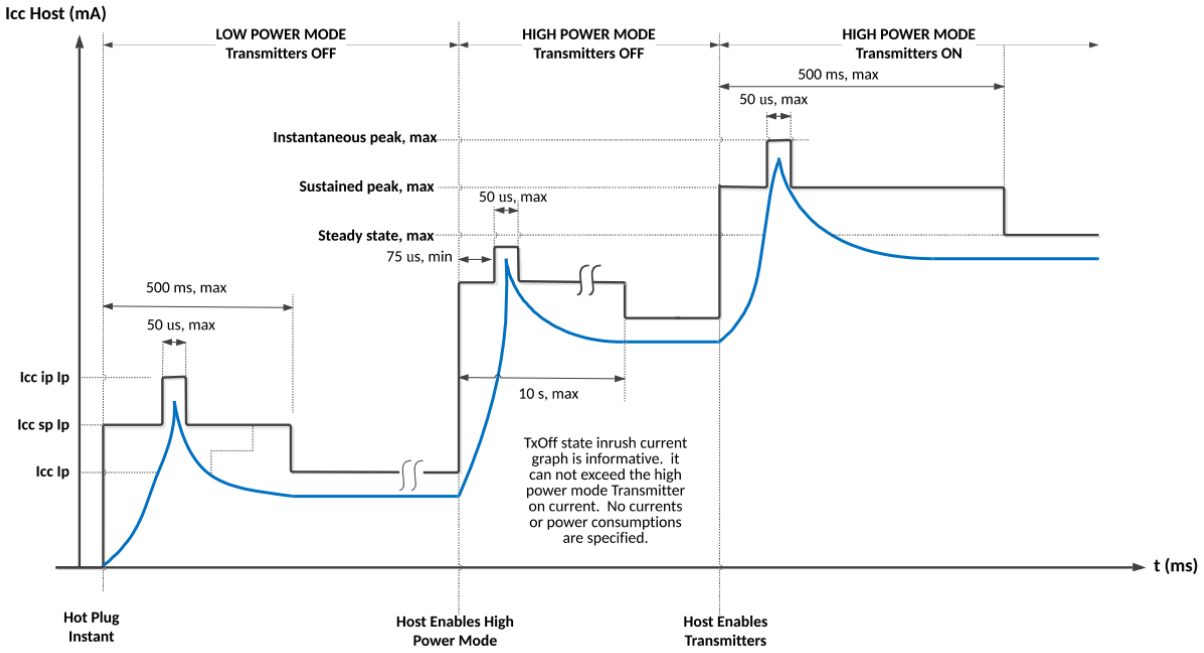

Figure 2. XR Instantaneous and Sustained Peak Currents

3.3 SGMII Interface Specification

The Open XR SGMII implementation is based on the Cisco System Serial-GMII Specification [7]. Only the 1000Mbps PHY is supported by Open XR module. Four pads are required for SGMII implementation; TXn/p and RXn/p as defined in previous hardware connector pad definition section. Open XR SGMII bus clock signal is from Rx recovered data clock so TXCLK and RXCLK are not required. The original SGMII specification was based on LVDS logic, XR is implemented using Current Mode Logic (CML) this is a deviation from the original specification.

Parameter	Symbol	Min	Typical	Max	Unit	Condition
Data Rate			1.25		Gbps	
Clock Tolerance		-100		+100	ppm	
Input Voltage Differential Swing	Vidpp	85		1200	mVdpp	
Input Impedance, Differential Integrated on Chip	Rin	80	100	120	Ohm	
Output Voltage Differential Swing	Vodpp	800	900	1200	mVdpp	
Output Impedance, Differential Integrated on Chip	Rout	80	100	120	Ohm	
External AC coupling is required for both input and output						

Table 5. SGMII Interface Hardware Requirement

Other Open XR SGMII interface PHY and MAC layer protocol signal mapping and control plane functions are as in the original SGMII specifications.

OIF is actively working on publishing E-SGMII as a high-speed interface between module communication and the host [8]. OXR is following the development and will adapt E-SGMII interface spec once it is standardized. The current SGMII requirement in this section is compatible with OIF E-SGMII project definition.

4. XR Host Client Interface support

4.1 Client Protocol Support

XR supports various types of Ethernet client services including 400GE, 200GE, 100GE, 50GE, and 25GE, also ITU OTN OTU4 client using 50~56Gbps PAM4 and 25 ~ 28Gbps NRZ modulations.

When running at 50~56Gbps per host electrical lane data rate for up to 400G data, XR optical module must comply with IEEE802.3 100GAUI-2, 200GAUI-4, and 400GAUI-8 C2M specification [2] for Ethernet applications. And XR module must comply with CEI-56G-VSR-PAM4 Specifications [3] for OTU4 application [4].

When running at 25~28Gbps per host electrical lane data rate for up to 200G data, XR optical module must comply with IEEE802.3 25GAUI and 100G CAUI-4 C2M specification [2] for Ethernet applications. And XR module must comply with CEI-28G-VSR Specifications [3] for OTU4 application [4].

5. Management Interface and Module Timing Requirement

Each formfactor has its specific management interface implementation specification and timing requirements for soft control and hardware control defined in the appropriate MSA documents. XR shall comply to those form factor specific MSA requirements with the exception of the following XR deviations listed Table 6 and Table 7.

5.1 QSFP-DD

Parameter	Symbol	Min	Max	Unit	Conditions
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (Optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted (Optional fast RxLOS is required for protection switching application. Not all XR requires this. Vendor can select fast mode for implementation)
Rx LOS Deassert Time	toff_los		100	ms	Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high
Tx Squelch Assert Time	ton_Txsq		NA		Time from loss of Tx input signal until the squelched output condition is reached. Not supported. Tx Squelch not supported.
Tx Squelch Deassert Time	toff_Txsq		NA		Time from resumption of Tx input signals until normal Tx output condition is reached. Not supported. Tx Squelch not supported
Tx Disable Assert Time	ton_txdis		3	ms	Time from the stop condition of the Tx Disable write sequence on I2C management interface until optical

					output falls below 10% of nominal power. (Compliant to QSFP-DD optional fast Tx disable mode)
Tx Disable De-assert Time	toff_txdis		400	ms	Time from Tx Disable bit cleared (value = 0b) until optical output rises above 90% of nominal.
Note1: All specifications in this table are for control over module Management Communication Interface. XR does not require QSFP-DD alternative hardware TxDIS and RxLOS pin implementation					

Table 6. QSFP-DD XR Optical Module Management Timing Requirement (with Deviation from Module MSAs)

5.2 CFP2

Parameter	Symbol	Min	Max	Unit	Conditions
Soft RX_LOS, RX_Network_LOL (LOF) assert time	t_Rx_los_lol_assert		150	ms	Time from RX_LOS, Rx_Network_LOL (LOF) condition occurred to module FAWS register 0xB01Dh is set and hardware Global Alarm pin is flagged
Soft RX_LOS, RX_Network_LOL (LOF) fast assert time (Optional fast mode)	t_Rx_los_lol_assert_f		10	ms	Time from RX_LOS, Rx_Network_LOL (LOF) condition occurred to module FAWS register 0xB01Dh is set and hardware Global Alarm pin is flagged
Soft RX_LOS, RX_Network_LOL (LOF) de-assert time	t_Rx_los_lol_deassert		150	ms	Time from RX_LOS, Rx_Network_LOL (LOF) condition cleared to module FAWS register 0xB01Dh is cleared
Soft Tx Squelch Assert Time			NA		Time from loss of Tx input signal until the squelched output condition is reached. Not supported by XR
Soft Tx Squelch De-assert Time			NA		Time from resumption of Tx input signals until normal Rx output condition is reached. Not supported by XR
Hardware Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	msec	This is a logical "OR" of associated MDIO alarm & status registers.
Hardware Global Alarm fast Assert Delay Time (Optional fast mode)	GLB_ALRMn_assert_f		10	msec	Fast Global Alarm assertion mode is required when fast Soft RX_LOS, RX_Network_LOL (LOF) assertion is required. It is to alert host to check module FAWS register for fault condition.
Hardware Global Alarm De-Assert Delay Time	GLB_ALRMn_deassert		150	msec	This is a logical "OR" of associated MDIO alarm & status registers.

Hardware Receiver Loss of Signal (Rx_LOS) Assert Time	t_loss_assert		1	msec	From receiver LOS condition occurs to the Rx_LOS pin is set to High
Hardware Receiver Loss of Signal (Rx_LOS) De-Assert Time	t_loss_deassert		15	msec	From receiver LOS condition removal to the Rx_LOS pin is set to Low
Hardware Transmitter Disabled (TX_DIS asserted)	t_deassert		10	msec	From Tx_Disable pin set by host to the time optical output reaches 10% of operating power level
Hardware Transmitter Enabled (TX_DIS de-asserted)	t_assert		45	msec	Time from Tx Disable pin De-asserted until CFP module enters the Tx-Turn-on State reaching >90% normal output power.

Table 7. CFP2 XR Optical Module Management Timing Requirement (with Deviation from Module MSAs)

6. Module Mechanical and Thermal Design Requirement (Form Factor Dependent)

XR module can be implemented in various form factors. XR modules shall follow form factor specific mechanical MSA specifications. Detail module dimensions and other mechanical properties can be found in module HW MSAs[5][1]. XR Module shall follow MSA guidelines. Each form factor has its limitation of power consumption. Module should have sufficient heat management design to support full operational temperature range specified by the device.

400G OpenXR module Pull tab color: Grey. PANTONE Cool Grey 11 or RAL 7022 Umbra Grey

References

[1] QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER – Rev 6.3
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